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EXAMINER	
CHEN, ERIC BRICE	

ART UNIT	PAPER NUMBER
1765	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,318	MUI ET AL.	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/28/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-13,15-23 and 25-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-13,15-23 and 25-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

2. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

3. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 8-11 and 16-19 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 7-8, 10, 12, and 19-20 of copending Application No. 10/666,317, Mui et al. (U.S. Patent Appl. Pub. No. 2005/0064714), in view of Tao et al. (U.S. Patent No. 6,620,631) ("Tao

I"), in further view of Tao et al. (U.S. Patent No. 6,242,350). This is a provisional obviousness-type double patenting rejection.

5. As to claim 8, Mui claims a method for controlling accuracy and repeatability of an etch process, comprising: (a) providing a batch of substrates, each substrate having a patterned mask formed on a film stack comprising at least one material layer (Application No. 10/666,317, Applicant's Amendments, filed Sept. 6, 2005, claim 1, page 6, line 3); (b) measuring dimensions of elements of the patterned mask on at least one substrate of the batch of substrates (claim 1, page 6, line 4); and (d) etching the at least one material layer on the at least one substrate (claim 1, page 6, lines 5-6); and (g) adjusting the process recipe of step (d) based on the measurements performed (claim 1, page 6, lines 7-8).

6. The claims of Mui fail to include the limitations of: (c) trimming the patterned mask on the at least one substrate using a process recipe based on the measurements performed at step (b); (f) measuring dimensions of etched structures formed on the at least one substrate during step; and (g) adjusting the process recipe of step (c) based on the measurements performed at step (f), as required by Applicants' claim 8. Tao I teaches a method of enhancing linewidth control and critical dimension during semiconductor fabrications (column 1, lines 22-26), including establishing a correlation relating the pattern masked layers with optical measurements, determining a deviation, and compensating for the deviation (column 8, lines 62-67), including adjusting the trimming of the patterned masking (column 9, lines 20-28). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to

include the steps of (c) trimming the patterned mask on the at least one substrate using a process recipe based on the measurements performed at step (b); (e) measuring dimensions of etched structures formed on the at least one substrate during step; and (f) adjusting the process recipe of step (c) based on the measurements performed at step (e). One who is skilled in the art would be motivated to adopt a process for enhancing linewidth control and critical dimension during semiconductor fabrications.

7. Mui does not claim (e), at least one of compacting/outgassing or removing at least a portion of post-etch residue formed on sidewalls of the etched structures. Tao II teaches that etching a polysilicon gate electrode (20) with HBr results in the deposition of polymer residue (24/26) (column 1, lines 44-51; Figure 2). Moreover, Tao II teaches that polymer residue (24/26) must be removed by a cleaning process (column 1, lines 49-51). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include step (e), at least one of compacting/outgassing or removing at least a portion of post-etch residue formed on sidewalls of the etched structures. One who is skilled in the art would be motivated to remove residues from a wafer after the completing of etching.

8. As to claim 9, Mui claims that the steps (b) and (f) use an optical measuring technique (claim 7, page 6, lines 24-25).

9. As to claim 10, the claims of Mui fail to include the limitation that the optical measuring technique is a scatterometric measuring technique. However, Tao I discloses that any optical method may be used for measuring patterned masked layers (column 8, lines 59-61). Moreover, Tao I teaches that a scatterometer apparatus has

been used successfully in characterizing the surface microelectronic device during fabrication (column 3, lines 1-11). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a scatterometric measuring technique. One who is skilled in the art would be motivated to use an optical technique, such scatterometric measuring, which has been previously demonstrated to accomplish the task of characterizing the surface of a microelectronic device.

10. As to claim 11, Mui claims that the steps (b) through (f) are performed using processing modules of a single substrate processing system (claim 8, page 6, lines 27-28).

11. As to claim 16, Mui claims a method for controlling accuracy and repeatability during formation of a gate structure of a field effect transistor (claim 12, page 7, lines 13-14), comprising: (a) providing a batch of substrates, each substrate having a patterned mask formed on a gate electrode layer of the gate structure (claim 12, page 7, lines 15-16); (b) measuring dimensions of elements of the patterned mask on at least one substrate of the batch of substrates (claim 12, page 7, line 17); (d) etching the gate electrode layer on the at least one substrate (claim 12, page 7, lines 18-19); and (f) adjusting the process recipe of step (d) based on the measurements performed (claim 12, page 7, lines 20-21).

12. The claims of Mui fail to include the limitations of: (c) trimming the patterned mask on the at least one substrate using a process recipe based on the measurements performed at step (b); (e) measuring dimensions of etched gate electrode structures formed on the at least one substrate during step (d); and adjusting the process recipe of

step (c) based on the measurements performed at step (f), as required by Applicants' claim 16. Tao I teaches a method of enhancing linewidth control and critical dimension during semiconductor fabrications (column 1, lines 22-26), including establishing a correlation relating the pattern masked layers with optical measurements, determining a deviation, and compensating for the deviation (column 8, lines 62-67), including adjusting the trimming of the patterned masking (column 9, lines 20-28). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the steps of (c) trimming the patterned mask on the at least one substrate using a process recipe based on the measurements performed at step (b); (e) measuring dimensions of etched gate electrode structures formed on the at least one substrate during step (d); and adjusting the process recipe of step (c) based on the measurements performed at step (f). One who is skilled in the art would be motivated to adopt a process for enhancing linewidth control and critical dimension during semiconductor fabrications.

13. Mui does not claim (e), at least one of compacting/outgassing or removing at least a portion of post-etch residue formed on sidewalls of the etched structures. Tao II teaches that etching a polysilicon gate electrode (20) with HBr results in the deposition of polymer residue (24/26) (column 1, lines 44-51; Figure 2). Moreover, Tao II teaches that polymer residue (24/26) must be removed by a cleaning process (column 1, lines 49-51). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include step (e), at least one of compacting/outgassing or removing at least a portion of post-etch residue formed on sidewalls of the etched

structures. One who is skilled in the art would be motivated to remove residues from a wafer after the completing of etching.

14. As to claim 17, Mui claims that the steps (b) and (f) use an optical measuring technique (claim 19, page 8, lines 13-14).

15. As to claim 18, the claims of Mui fail to include the limitation that the optical measuring technique is a scatterometric measuring technique. However, Tao I discloses that any optical method may be used for measuring patterned masked layers (column 8, lines 59-61). Moreover, Tao I teaches that a scatterometer apparatus has been used successfully in characterizing the surface microelectronic device during fabrication (column 3, lines 1-11). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a scatterometric measuring technique. One who is skilled in the art would be motivated to use an optical technique, such scatterometric measuring, which has been previously demonstrated to accomplish the task of characterizing the surface of a microelectronic device.

16. As to claim 19, Mui claims that the steps (b) through (f) are performed using processing modules of a single substrate processing system (claim 20, page 8, lines 16-17).

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

19. Claims 8-13, 15-23, and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tao I, in view of Tao II.

20. As to claim 8, Tao I discloses a method for controlling accuracy and repeatability of an etch process, comprising: (a) providing a batch of substrates, each substrate (10) (column 6, lines 37-41) having a patterned mask (14a/14b/14c/14d/14e) (column 7, lines 35-37) formed on a film stack comprising at least one material layer (12) (column 6, lines 34-36); (b) measuring dimensions of elements of the patterned mask (14a/14b/14c/14d/14e) on at least one substrate (10) (column 8, lines 50-61) of the batch of substrates (column 8, lines 62-67); (c) trimming the patterned mask (14a/14b/14c/14d/14e) (column 9, lines 20-28) on the at least one substrate using a process recipe based on the measurements performed at step (b) (column 8, lines 62-67; column 9, lines 1-15); (d) etching the at least one material layer on the at least one substrate (column 9, lines 1-4); (e) measuring dimensions of etched structures formed on the at least one substrate during step (d) (column 9, lines 4-12); and (f) adjusting the

process recipe of step (c) (column 9, lines 11-15, lines 26-28) or/and the process recipe of step (d) based on the measurements performed at step (f) (column 9, lines 4-15).

21. Tao I does not expressly discloses step (e), at least one of compacting/outgassing or removing at least a portion of post-etch residue formed on sidewalls of the etched structures. Tao II teaches that etching a polysilicon gate electrode (20) with HBr results in the deposition of polymer residue (24/26) (column 1, lines 44-51; Figure 2). Moreover, Tao II teaches that polymer residue (24/26) must be removed by a cleaning process (column 1, lines 49-51). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include step (e), at least one of compacting/outgassing or removing at least a portion of post-etch residue formed on sidewalls of the etched structures. One who is skilled in the art would be motivated to remove residues from a wafer after the completing of etching.

22. As to claim 9, Tao I discloses that the steps (b) and (f) use an optical measuring technique (column 8, lines 50-61).

23. As to claims 10, Tao I does not expressly disclose that the optical measuring technique is a scatterometric measuring technique. However, Tao I discloses that any optical method may be used (column 8, lines 59-61). Moreover, Tao I teaches that a scatterometer apparatus has been used successfully in characterizing the surface microelectronic device during fabrication (column 3, lines 1-11). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a scatterometric measuring technique. One who is skilled in the art would be motivated to use an optical technique, such scatterometric measuring, which has been

previously demonstrated to accomplish the task of characterizing the surface of a microelectronic device.

24. As to claim 11, Tao I discloses that steps (b) through (f) are performed using processing modules of a single substrate processing system (column 5, lines 38-44).

25. As to claim 12, Tao I discloses that the step (g) further comprises: modifying a time duration or process parameters for trimming the patterned mask (column 9, lines 20-28).

26. As to claim 13, Tao I discloses that the step (g) further comprises: modifying a time duration or process parameters for etching the material layer (column 9, lines 4-15).

27. As to claims 15, Tao I does not expressly disclose thinning the post-etch residue to a thickness of less than about 10 nm. Tao II teaches that etching polysilicon with HBr results in the deposition of polymer residue (56/58/60) (column 5, lines 8-14; Figure 4). Moreover, Tao II teaches that the polymer reside can be removed by dry etching with nitrogen (N_2), oxygen (O_2) and hydrogen (H_2) (column 6, lines 64-67). However, this etching step also etches the gate oxide (column 5, lines 18-24). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to thin the post-etch residue to a thickness of less than about 10 nm. One who is skilled in the art would be motivated to remove the residue, but not overetch the gate oxide.

28. As to claim 16, Tao I discloses a method for controlling accuracy and repeatability during formation of a gate structure of a field effect transistor (column 5, lines 56-63), comprising: (a) providing a batch of substrates, each substrate (10) having

a patterned mask (14a/14b/14c/14d/14e) (column 7, lines 35-37) formed on a gate electrode layer of the gate structure; (b) measuring dimensions of elements of the patterned mask (12) (column 7, lines 21-31; Figure 1) on at least one substrate of the batch of substrates (column 8, lines 62-67); (c) trimming the patterned mask (14a/14b/14c/14d/14e) (column 9, lines 20-28) on the at least one substrate using a process recipe based on the measurements performed at step (b) (column 8, lines 62-67; column 9, lines 1-15); (d) etching the gate electrode layer on the at least one substrate (column 9, lines 1-4); (f) measuring dimensions of etched gate electrode structures formed on the at least one substrate during step (g) (column 9, lines 4-12); and (f) adjusting the process recipe of step (c) (column 9, lines 11-15, lines 26-28) or/and the process recipe of step (d) based on the measurements performed at step (f) (column 9, lines 4-15).

29. Tao I does not expressly discloses step (e), at least one of compacting/outgassing or removing at least a portion of post-etch residue formed on sidewalls of the etched structures. Tao II teaches that etching a polysilicon gate electrode (20) with HBr results in the deposition of polymer residue (24/26) (column 1, lines 44-51; Figure 2). Moreover, Tao II teaches that polymer residue (24/26) must be removed by a cleaning process (column 1, lines 49-51). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include step (e), at least one of compacting/outgassing or removing at least a portion of post-etch residue formed on sidewalls of the etched structures. One who is skilled in the art would be motivated to remove residues from a wafer after the completing of etching.

30. As to claim 17, Tao I discloses that the steps (b) and (f) use an optical measuring technique (column 8, lines 50-61).

31. As to claim 18, Tao I does not expressly disclose that the optical measuring technique is a scatterometric measuring technique. However, Tao I discloses that any optical method may be used (column 8, lines 59-61). Moreover, Tao I teaches that a scatterometer apparatus has been used successfully in characterizing the surface microelectronic device during fabrication (column 3, lines 1-11). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a scatterometric measuring technique. One who is skilled in the art would be motivated to use an optical technique, such scatterometric measuring, which has been previously demonstrated to accomplish the task of characterizing the surface of a microelectronic device.

32. As to claim 19, Tao I discloses that the steps (b) through (f) are performed using processing modules of a single substrate processing system (column 5, lines 38-44).

33. As to claim 20, Tao I discloses that the step (g) further comprises: modifying a time duration or process parameters for trimming the patterned mask (column 9, lines 20-28).

34. As to claim 21, Tao I discloses that the step (g) further comprises: modifying a time duration or process parameters for etching the material layer (column 9, lines 4-15).

35. As to claim 22, Tao I discloses that the gate electrode layer (12) comprises doped polysilicon (column 7, lines 21-25).

36. As to claim 23, Tao I does not expressly disclose that the step (d) further comprises: providing HBr and Cl_2 at a flow ratio HBr:Cl_2 in a range from 1:15 to 15:1. However, Tao II discloses a method of etching polysilicon layer (46) overlying gate oxide (42) (Figure 3) with HBr and Cl_2 at a flow ratio HBr:Cl_2 in a range from 1:15 to 15:1 (column 4, lines 31-54). Moreover, Tao II teaches that the flow ratio HBr:Cl_2 is varied in order to achieve a desired polysilicon/oxide selectivity, to avoid overetching the gate oxide (42) (column 4, lines 44-49). Therefore, it would have obvious to one of ordinary skill in the art to provide HBr and Cl_2 at a flow ratio HBr:Cl_2 in a range from 1:15 to 15:1. One who is skilled in the art would adopt an etching method that avoids overetching of an underlying gate oxide.

37. As to claims 25, Tao I does not expressly disclose thinning the post-etch residue to a thickness of less than about 10 nm. Tao II teaches that etching polysilicon with HBr results in the deposition of polymer residue (56/58/60) (column 5, lines 8-14; Figure 4). Moreover, Tao II teaches that the polymer reside can be removed by dry etching with nitrogen (N_2), oxygen (O_2) and hydrogen (H_2) (column 6, lines 64-67). However, this etching step also etches the gate oxide (column 5, lines 18-24). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to thin the post-etch residue to a thickness of less than about 10 nm. One who is skilled in the art would be motivated to remove the residue, but not overetch the gate oxide.

38. As to claim 26, Tao I does not expressly disclose using a plasma comprising one or more gases selected from the group consisting of nitrogen (N_2), oxygen (O_2) and hydrogen (H_2). Tao II teaches that etching polysilicon with HBr results in the deposition

of polymer residue (56/58/60) (column 5, lines 8-14; Figure 4). Moreover, Tao II teaches that the polymer reside can be removed by dry etching with nitrogen (N_2), oxygen (O_2) and hydrogen (H_2) (column 6, lines 64-67). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to using a plasma comprising one or more gases selected from the group consisting of nitrogen (N_2), oxygen (O_2) and hydrogen (H_2). One who is skilled in the art would be motivated to remove polymer residue after the etching polysilicon with HBr.

39. As to claim 27, Tao II discloses providing nitrogen (N_2) and hydrogen (H_2) at a N_2:H_2 flow ratio in a range from 3:1 to 100% of N_2 (column 7, lines 1-4); maintaining the substrate at a temperature between about 200 and 350 degrees Celsius (column 7, lines 27-28; Table II); applying power to an inductively coupled power source between about 1000 and 7000 W (column 7, lines 23-24; Table II); and maintaining a chamber pressure between about 500 and 2000 mTorr (column 7, lines 22-23; Table II).

Response to Arguments

40. Applicants' intentions of filing a Terminal Disclaimer once either of the applications is allowed has been noted (Applicants' Remarks, page 6). Upon the filing of a proper Terminal Disclaimer, the provisional rejection of claims 8-11 and 16-19 under the judicially-created doctrine of obviousness-type double patenting will be withdrawn.

41. Applicants' arguments (Applicants' Remarks, page 7, paragraph 3), filed Sept. 28, 2005, with respect to the rejection of claims 8-9, 11-14, 16-17, 19-22, and 24 under

35 U.S.C. 102(e) has being anticipated by Tao I have been fully considered and are persuasive. Applicants have pointed out that Tao I teaches the formation of a polymer layer rather than removal (page 7, paragraph 3). Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Tao II.

42. Applicants' arguments (Applicants' Remarks, pages 7-8), filed Sept. 28, 2005, with respect to the rejection of claims 10 and 18 under 35 U.S.C. 103(a) has being unpatentable over Tao I have been fully considered and are persuasive, as discussed above. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Tao II.

43. Applicants' arguments (Applicants' Remarks, pages 7-8), filed Sept. 28, 2005, with respect to the rejection of claims 15, 23, and 25-27 under 35 U.S.C. 103(a) has being unpatentable over Tao I, in view of Tao II, have been fully considered and are persuasive, in part. A discussion of Tao I was previously discussed. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Tao II.

44. However, Applicants' arguments with respect to the motivation to combine Tao I with Tao II have been have been fully considered, but they are not persuasive. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Tao I teaches forming a polymer upon the sidewalls of patterned masking layers

(14A/14B/14C/14D/14E) (column 9, lines 20-38). Moreover, Tao II teaches that sidewall polymers (24) play an important role of protected the wall of the etched structure, enabling a sidewall profile (column 1, lines 64-67; Figure 2). However, Tao II further teaches that after etching has been completed, all residues of all various types must be removed (column 1, lines 49-51), including sidewall polymer (24) (column 1, lines 58-59). In other words, formation of a sidewall polymer is beneficial during etching to preserve the vertical profile, but after etching has been completed, all polymer residues must be removed. Therefore, sufficient motivation exists to combine the Tao I and Tao II references.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC

EBC
Nov. 9, 2005

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER